



1. Description

1.1. Project

| | |
|-----------------|--------------------------------|
| Project Name | F439_CPP_TX-RX_LoRa_Project_01 |
| Board Name | NUCLEO-F439ZI |
| Generated with: | STM32CubeMX 6.14.1 |
| Date | 05/06/2026 |

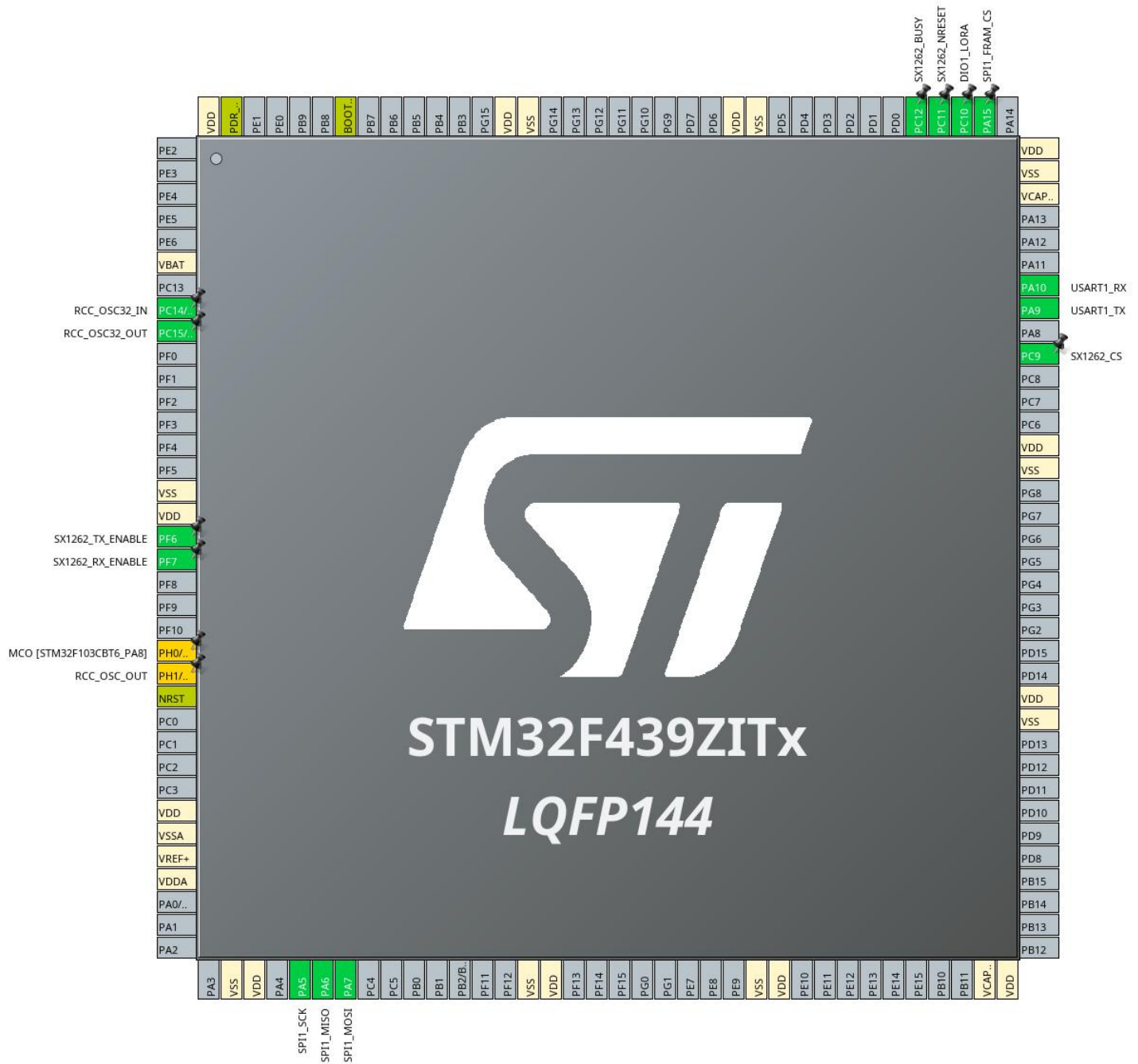
1.2. MCU

| | |
|----------------|---------------|
| MCU Series | STM32F4 |
| MCU Line | STM32F429/439 |
| MCU name | STM32F439ZITx |
| MCU Package | LQFP144 |
| MCU Pin number | 144 |

1.3. Core(s) information

| | |
|---------|---------------|
| Core(s) | Arm Cortex-M4 |
|---------|---------------|

2. Pinout Configuration



3. Pins Configuration

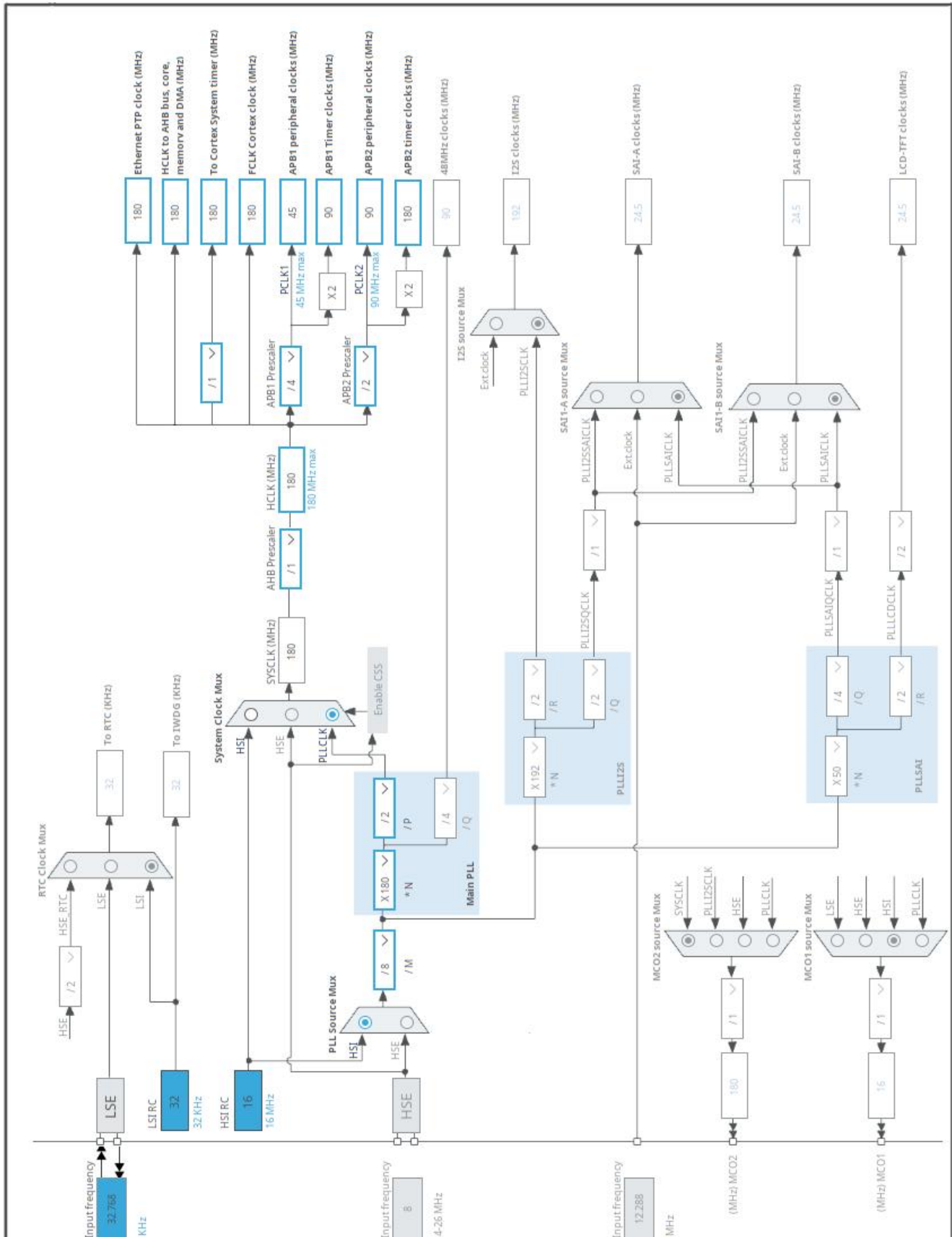
| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|----------------------------|
| 6 | VBAT | Power | | |
| 8 | PC14/OSC32_IN | I/O | RCC_OSC32_IN | |
| 9 | PC15/OSC32_OUT | I/O | RCC_OSC32_OUT | |
| 16 | VSS | Power | | |
| 17 | VDD | Power | | |
| 18 | PF6 * | I/O | GPIO_Output | SX1262_TX_ENABLE |
| 19 | PF7 * | I/O | GPIO_Output | SX1262_RX_ENABLE |
| 23 | PH0/OSC_IN ** | I/O | RCC_OSC_IN | MCO [STM32F103CBT6_PA8] |
| 24 | PH1/OSC_OUT ** | I/O | RCC_OSC_OUT | |
| 25 | NRST | Reset | | |
| 30 | VDD | Power | | |
| 31 | VSSA | Power | | |
| 32 | VREF+ | Power | | |
| 33 | VDDA | Power | | |
| 38 | VSS | Power | | |
| 39 | VDD | Power | | |
| 41 | PA5 | I/O | SPI1_SCK | |
| 42 | PA6 | I/O | SPI1_MISO | |
| 43 | PA7 | I/O | SPI1_MOSI | |
| 51 | VSS | Power | | |
| 52 | VDD | Power | | |
| 61 | VSS | Power | | |
| 62 | VDD | Power | | |
| 71 | VCAP_1 | Power | | |
| 72 | VDD | Power | | |
| 83 | VSS | Power | | |
| 84 | VDD | Power | | |
| 94 | VSS | Power | | |
| 95 | VDD | Power | | |
| 99 | PC9 * | I/O | GPIO_Output | SX1262_CS |
| 101 | PA9 | I/O | USART1_TX | |
| 102 | PA10 | I/O | USART1_RX | |
| 106 | VCAP_2 | Power | | |
| 107 | VSS | Power | | |
| 108 | VDD | Power | | |

| Pin Number LQFP144 | Pin Name (function after reset) | Pin Type | Alternate Function(s) | Label |
|-----------------------|---------------------------------------|----------|--------------------------|---------------|
| 110 | PA15 * | I/O | GPIO_Output | SPI1_FRAM_CS |
| 111 | PC10 | I/O | GPIO_EXTI10 | DIO1_LORA |
| 112 | PC11 * | I/O | GPIO_Output | SX1262_NRESET |
| 113 | PC12 * | I/O | GPIO_Input | SX1262_BUSY |
| 120 | VSS | Power | | |
| 121 | VDD | Power | | |
| 130 | VSS | Power | | |
| 131 | VDD | Power | | |
| 138 | BOOT0 | Boot | | |
| 143 | PDR_ON | Reset | | |
| 144 | VDD | Power | | |

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



1. Power Consumption Calculator report

1.1. Microcontroller Selection

| | |
|-----------|---------------|
| Series | STM32F4 |
| Line | STM32F429/439 |
| MCU | STM32F439ZITx |
| Datasheet | DS9484_Rev10 |

1.2. Parameter Selection

| | |
|-------------|-----|
| Temperature | 25 |
| Vdd | 3.3 |

1.3. Battery Selection

| | |
|-------------------|-----------------|
| Battery | Li-SOCL2(A3400) |
| Capacity | 3400.0 mAh |
| Self Discharge | 0.08 %/month |
| Nominal Voltage | 3.6 V |
| Max Cont Current | 100.0 mA |
| Max Pulse Current | 200.0 mA |
| Cells in series | 1 |
| Cells in parallel | 1 |

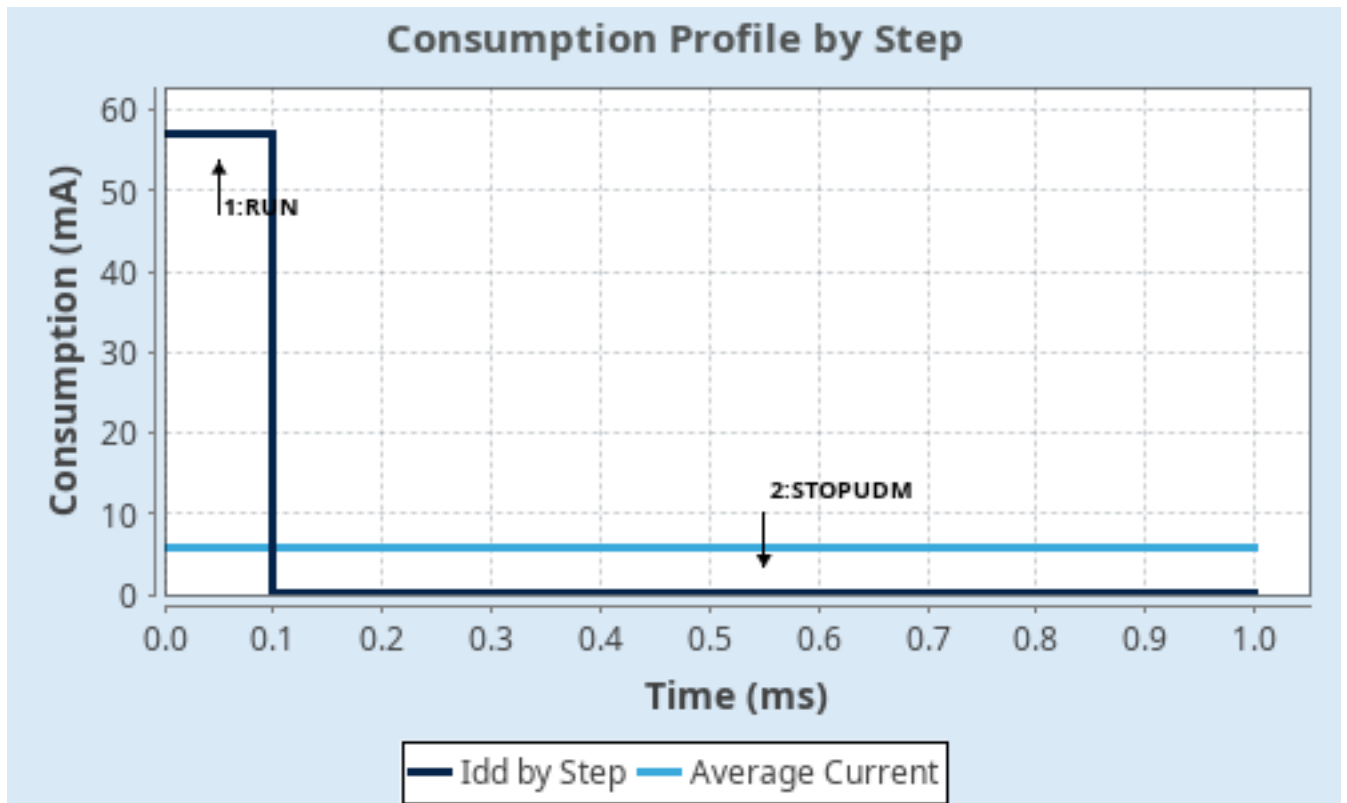
1.4. Sequence

| | | |
|-------------------------------|-------------|---------------------------|
| Step | Step1 | Step2 |
| Mode | RUN | STOP UDM (Under Drive) |
| Vdd | 3.3 | 3.3 |
| Voltage Source | Battery | Battery |
| Range | Scale1-High | No Scale |
| Fetch Type | FLASH | n/a |
| CPU Frequency | 180 MHz | 0 Hz |
| Clock Configuration | HSE PLL | Regulator LP Flash-PwrDwn |
| Clock Source Frequency | 4 MHz | 0 Hz |
| Peripherals | | |
| Additional Cons. | 0 mA | 0 mA |
| Average Current | 57 mA | 100 μ A |
| Duration | 0.1 ms | 0.9 ms |
| DMIPS | 225.0 | 0.0 |
| Ta Max | 97.48 | 104.99 |
| Category | In DS Table | In DS Table |

1.5. Results

| | | | |
|---------------|-------------------|-----------------|-------------|
| Sequence Time | 1 ms | Average Current | 5.79 mA |
| Battery Life | 24 days, 10 hours | Average DMIPS | 225.0 DMIPS |

1.6. Chart



2. Software Project

2.1. Project Settings

| Name | Value |
|-----------------------------------|---|
| Project Name | F439_CPP_TX-RX_LoRa_Project_01 |
| Project Folder | /home/johng/workbench6/F439_CPP_TX-RX_LoRa_Project_01 |
| Toolchain / IDE | STM32CubeIDE |
| Firmware Package Name and Version | STM32Cube FW_F4 V1.28.3 |
| Application Structure | Advanced |
| Generate Under Root | Yes |
| Do not generate the main() | No |
| Minimum Heap Size | 0x200 |
| Minimum Stack Size | 0x400 |

2.2. Code Generation Settings

| Name | Value |
|---|---------------------------------------|
| STM32Cube MCU packages and embedded software | Copy only the necessary library files |
| Generate peripheral initialization as a pair of '.c/.h' files | No |
| Backup previously generated files when re-generating | Yes |
| Keep User Code when re-generating | Yes |
| Delete previously generated files when not re-generated | Yes |
| Set all free pins as analog (to optimize the power consumption) | No |
| Enable Full Assert | Yes |

2.3. Advanced Settings - Generated Function Calls

| Rank | Function Name | Peripheral Instance Name |
|------|---------------------|--------------------------|
| 1 | SystemClock_Config | RCC |
| 2 | MX_GPIO_Init | GPIO |
| 3 | MX_SPI1_Init | SPI1 |
| 4 | MX_USART1_UART_Init | USART1 |
| 5 | MX_TIM3_Init | TIM3 |
| 6 | MX_CRYP_Init | CRYP |

3. Peripherals and Middlewares Configuration

3.1. CRYPT

mode: Activated

3.1.1. Parameter Settings:

Algorithm:

Data encryption algorithm

AES CTR *

Parameters:

Data type

32b(no swapping)

Key size

128b

Encryption/Decryption key

00000000 00000000 00000000 00000000

Initialization vector

00000000 00000000 00000000 00000000

Data width unit

Byte *

3.2. RCC

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)

3.3

Instruction Cache

Enabled

Prefetch Buffer

Enabled

Data Cache

Enabled

Flash Latency(WS)

5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value

16

TIM Prescaler Selection

Disabled

HSE Startup Timeout Value (ms)

100

LSE Startup Timeout Value (ms)

5000

Power Parameters:

Power Regulator Voltage Scale

Power Regulator Voltage Scale 1

Power Over Drive

Enabled

3.3. SPI1

Mode: Full-Duplex Master

3.3.1. Parameter Settings:

Basic Parameters:

| | |
|--------------|-----------|
| Frame Format | Motorola |
| Data Size | 8 Bits |
| First Bit | MSB First |

Clock Parameters:

| | |
|---------------------------|--------------------------|
| Prescaler (for Baud Rate) | 64 * |
| Baud Rate | 1.40625 MBits/s * |
| Clock Polarity (CPOL) | Low |
| Clock Phase (CPHA) | 1 Edge |

Advanced Parameters:

| | |
|-----------------|----------|
| CRC Calculation | Disabled |
| NSS Signal Type | Software |

3.4. SYS

Timebase Source: SysTick

3.5. TIM3

Clock Source : Internal Clock

3.5.1. Parameter Settings:

Counter Settings:

| | |
|---|-----------------|
| Prescaler (PSC - 16 bits value) | 90 - 1 * |
| Counter Mode | Up |
| Counter Period (AutoReload Register - 16 bits value) | 65535 |
| Internal Clock Division (CKD) | No Division |
| auto-reload preload | Disable |

Trigger Output (TRGO) Parameters:

| | |
|-----------------------------|--|
| Master/Slave Mode (MSM bit) | Disable (Trigger input effect not delayed) |
| Trigger Event Selection | Reset (UG bit from TIMx_EGR) |

3.6. USART1

Mode: Asynchronous

3.6.1. Parameter Settings:

Basic Parameters:

| | |
|-------------|---------------------------|
| Baud Rate | 19200 * |
| Word Length | 8 Bits (including Parity) |
| Parity | None |
| Stop Bits | 1 |

Advanced Parameters:

| | |
|----------------|----------------------|
| Data Direction | Receive and Transmit |
| Over Sampling | 16 Samples |

* User modified value

4. System Configuration

4.1. GPIO configuration

| IP | Pin | Signal | GPIO mode | GPIO pull/up pull down | Max Speed | User Label |
|-----------------------|----------------|---------------|--|-----------------------------|-------------|-------------------------|
| RCC | PC14/OSC32_IN | RCC_OSC32_IN | n/a | n/a | n/a | |
| | PC15/OSC32_OUT | RCC_OSC32_OUT | n/a | n/a | n/a | |
| SPI1 | PA5 | SPI1_SCK | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PA6 | SPI1_MISO | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PA7 | SPI1_MOSI | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| USART1 | PA9 | USART1_TX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| | PA10 | USART1_RX | Alternate Function Push Pull | No pull-up and no pull-down | Very High * | |
| Single Mapped Signals | PH0/OSC_IN | RCC_OSC_IN | n/a | n/a | n/a | MCO [STM32F103CBT6_PA8] |
| | PH1/OSC_OUT | RCC_OSC_OUT | n/a | n/a | n/a | |
| GPIO | PF6 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | SX1262_TX_ENABLE |
| | PF7 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | SX1262_RX_ENABLE |
| | PC9 | GPIO_Output | Output Push Pull | Pull-up * | Very High * | SX1262_CS |
| | PA15 | GPIO_Output | Output Push Pull | Pull-up * | Very High * | SPI1_FRAM_CS |
| | PC10 | GPIO_EXTI10 | External Interrupt Mode with Rising edge trigger detection | No pull-up and no pull-down | n/a | DIO1_LORA |
| | PC11 | GPIO_Output | Output Push Pull | No pull-up and no pull-down | Very High * | SX1262_NRESET |
| | PC12 | GPIO_Input | Input mode | No pull-up and no pull-down | n/a | SX1262_BUSY |

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

| Interrupt Table | Enable | Preenmption Priority | SubPriority |
|---|--------|----------------------|-------------|
| Non maskable interrupt | true | 0 | 0 |
| Hard fault interrupt | true | 0 | 0 |
| Memory management fault | true | 0 | 0 |
| Pre-fetch fault, memory access fault | true | 0 | 0 |
| Undefined instruction or illegal state | true | 0 | 0 |
| System service call via SWI instruction | true | 0 | 0 |
| Debug monitor | true | 0 | 0 |
| Pendable request for system service | true | 0 | 0 |
| System tick timer | true | 0 | 0 |
| EXTI line[15:10] interrupts | true | 0 | 0 |
| PVD interrupt through EXTI line 16 | unused | | |
| Flash global interrupt | unused | | |
| RCC global interrupt | unused | | |
| TIM3 global interrupt | unused | | |
| SPI1 global interrupt | unused | | |
| USART1 global interrupt | unused | | |
| CRYP global interrupt | unused | | |
| FPU global interrupt | unused | | |

4.3.2. NVIC Code generation

| Enabled interrupt Table | Select for init sequence ordering | Generate IRQ handler | Call HAL handler |
|---|-----------------------------------|----------------------|------------------|
| Non maskable interrupt | false | true | false |
| Hard fault interrupt | false | true | false |
| Memory management fault | false | true | false |
| Pre-fetch fault, memory access fault | false | true | false |
| Undefined instruction or illegal state | false | true | false |
| System service call via SWI instruction | false | true | false |
| Debug monitor | false | true | false |
| Pendable request for system service | false | true | false |
| System tick timer | false | true | true |
| EXTI line[15:10] interrupts | false | true | true |

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Multimedia

Security

Computing

DMA

TIM3



SPI1



CRYP



GPIO



USART1



NVIC



RCC



SYS



6. Docs & Resources

| Type | Link |
|-------------------------|---|
| BSDL files | https://www.st.com/resource/en/bsdl_model/stm32f427-437_429-439_bsdl.zip |
| IBIS models | https://www.st.com/resource/en/ibis_model/stm32f427-437_429-439_ibis.zip |
| System View Description | https://www.st.com/resource/en/svd/stm32f4-svd.zip |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf |
| Presentations | https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf |
| Brochures | https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf |
| Brochures | https://www.st.com/resource/en/brochure/expansion-boards-for-intelligent-power-switches.pdf |
| Flyers | https://www.st.com/resource/en/flyer/flstm32nucleo.pdf |
| Flyers | https://www.st.com/resource/en/flyer/flstm32trust.pdf |
| Flyers | https://www.st.com/resource/en/flyer/flstm32gui.pdf |
| Product Certifications | https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf |
| Security Bulletin | https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf |
| Application Notes | https://www.st.com/resource/en/application_note/an1709-emc-design- |

guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2945-stm8s-and-stm32-mcus-a-consistent-832bit-product-line-for-painless-migration-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3070-managing-the-driver-enable-signal-for-rs485-and-iolink-communications-with-the-stm32s-usart-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3155-usart-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

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Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

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- Application Notes https://www.st.com/resource/en/application_note/an4547-migrating-from-stm32f407xx417xx-to-stm32f427xx429xx437xx439xx-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4640-peripherals-interconnections-on-stm32f4057xx-stm32f4157xx-stm32f42xxx-stm32f43xxx-stm32f446xx-and-stm32f469479xx-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4658-migration-of-applications-from-stm32f429439-lines-to-stm32f446-line-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4660-migration-of-microcontroller-applications-from-stm32f42xxx43xxx-devices-to-stm32f7-series-devices-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4675-migration-of-microcontroller-applications-from-stm32f42xxxstm32f43xxx-to-stm32f469xxstm32f479xx-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4739-stm32cube-firmware-examples-for-stm32f4-series-stmicroelectronics.pdf
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